Bi-weekly Status Report 3
Senior Design, December 2020, Team 14

Introduction of Real-World Signals and Systems into ECpE DSP Laboratory Curriculum

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Progress Summary:
Over the last two weeks, we completed Rev 1 of our Design Doc, began work on EE 224 lab documents, set up the Zybo firmware with an initial commit to Git, designed Rev 1 of the CyDAQ's DAC, and continued working on the GUI. We also obtained and organized all of the course and lab documents relevant to this project–namely EE 224 labs, EE 324 labs, and course syllabi. We also created our LaTeX lab manual template, to be used when creating our new lab manuals.

Individual Contributions by Team Member:

- **Brady Anderson (Biweekly: 13; Cumulative: 37)**
  - Completed first revision of the Design Document™
  - Created Excel spreadsheet documenting CyDAQ command string formats
    - Allows developers to test the CyDAQ without the front-end GUI
  - Fixed Vivado project errors
  - Debugged Zybo UART connection
    - Fixed BSP UART target - should target UART1 on Zybo instead of UART0
    - Fixed UART device macros in SDK project
    - Updated compiler flags - may be able to revert to reduce compiled size
  - Successfully sampled test data using the CyDAQ board and GUI
  - Committed firmware to Git
- **Sam Burnett (Bi-weekly: 14, Cumulative: 39)**
  - Completed first revision of the Design Document™
  - Researched communications interface for FPGA integration of digital to analog converter(DAC)
  - Selected parts for first Peripheral Module (PMOD) draft for integrated DAC
  - Drafted circuit schematic diagram for DAC PMOD
  - Designed printed circuit board (PCB) layout for DAC PMOD
  - Conducted design review with teammates for DAC PMOD PCB
- **Mitchell Hoppe (Weekly: 13.5; Cumulative: 38.0)**
  - Completed first revision of the Design Document™
  - Updated website to include more reports and the Design Document
  - Worked on the UI for error checking of parameters
    - The CLI will check if the given parameters are valid options, and spell check if anything is spelled wrong.

    - Worked on the Bi-Weekly Status Report 3
- **Max Kiley (Biweekly: 10; Cumulative: 34)**
    - Completed first revision of the Design Document™
    - Reviewed Fourier Series and other EE 224 concepts.
    - Demoed a FS lab for EE224
    - Reviewed Matlab concepts and syntax
    - Started working on a noise reduction lab for EE224
- **Emily Lagrant (Biweekly: 14; Cumulative: 39)**
    - Completed first revision of the Design Document™
    - Reviewed 224 concepts and worked with 225 learning objectives
    - Researched potentially useful Matlab syntax
    - Began work on 224 lab prototype for Noise Reduction Lab
        - Developed .wav file and added white noise to be filtered out by a low pass filter
        - Finished planning the lab work
        - Started making lab in LaTeX template
- **Isaac Rex (Bi-Weekly: $\sum_{n=-\infty}^{\infty} 2u[n] - 2u[n-6] + \frac{5}{2}\delta[n]$; Cumulative: 40)**
    - Completed first revision of the Design Document™
    - Obtained EE 324 labs and pushed to git
    - Obtained Syllabi for classes and pushed to git
    - Research DSP labs from UC Berkeley
    - Created a LaTeX lab template to be used for all lab manuals
    - Completed initial system model of ball and plank for controls lab
    - Started obtaining parts for physical system build
    - Shared sensor data an analysis scheme with Dr. Dickerson for CprE 288 lab tie-in
    - Worked with initial Matlab prototype for EE 224 square wave construction lab

<u>Pending Issues:</u>

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<u>Plans:</u>

- Isaac:
    - Complete first draft of CyDAQ introduction lab
        - To be completed by March 6th
    - Complete a prototype for square wave filter and reconstruction lab
    - Continue researching UC Berkeley labs for implementation ideas
    - Start brainstorming second-half semester labs
    - Start physical build of ball and plank system for controls lab
- Emily:
    - Continue writing Noise Reduction Lab
    - Begin writing Aliasing lab

- Brady:
    - Test CyDAQ UART on different Zybo boards - confirm that the issue is with the design, and not the test unit
    - Investigate FreeRTOS and consider implementation strategies
    - Test Sam's PWM intuition lab with prototype PMOD
- Sam:
    - Design PCB for passive XACD level shifter
    - Write pre-lab and lab document for PWM intuition
    - Generate bill-of-materials for PMOD DAC
    - Order rev 1 of PMOD DAC
    - Assemble and test PMOD DAC

- Max
    - Continue to work on the Noise Reduction labs for EE 224.
    - Continue to demo the Fourier Series lab for EE 224.
    - Familiarize myself with EE 224 concepts and Matlab fundamentals.
- Mitch
    - Continue work on the UI for parameter checking and commands for debugging
    - Work on the GUI to improve user experience
    - Update the website to keep it up to date with documents and reports